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(54) [Title of the Invention] Inverter circuit

(57) [Abstract]

[Object] It is an object to provide an inverter circuit capable of realizing stable performance without influence of variations in a characteristic value of an individual inverter.

[Constitution] It is configured by being connected with a plurality of inverters INV1, INV2, ..., INVn in parallel between an input terminal VIN and an output terminal VOUT.

[Scope of Claim]

[Claim 1] An inverter circuit characterized by providing a plurality of unit inverter circuits in parallel between an input terminal and an output terminal

[Claim2] The inverter circuit according to claim 1, characterized in that the unit inverter circuit comprises a C-MOS inverter configured by a serially-connected pMOS type FET and nMOS type FET.

[Claim 3] The inverter circuit according to claim 1, characterized in that a plurality of unit inverter circuits for an inverter circuit are disposed closely and two-dimensionally, and unit inverters in a corresponding position in different inverter circuits is adjacently disposed one another on an LSI substrate.

[Detailed Description of the Invention]

[0001]

[Industrial Field of the Invention] The present invention relates to an inverter circuit and more specifically to an inverter circuit using a plurality of C-MOS inverters.

[0002]

[Prior Art] In an integrated circuit (IC), a C-MOS inverter configured by connecting a pMOS type FET and an nMOS type FET serially has been used conventionally.

[0003]

[Problem to be Solved by the Invention] However, an inverter circuit configured by using one above-mentioned conventional inverter has a problem that variations are generated due to variations in performance of FETs configuring an inverter in setting a

threshold voltage or the like, and stability performance is not assured.

[0004]

[Object of the invention] The present invention is made in view of solving the above-mentioned problem in prior art. It is an object of the invention to provide an inverter circuit capable of realizing stable performance without influence of variations in a characteristic value of an individual inverter.

[0005]

[Means for Solving the Problem] An inverter circuit according to the present invention is characterized in that a plurality of unit inverter circuit is provided between an input terminal and an output terminal in parallel to realize the above object.

[0006]

[Embodiment] Hereinafter, an embodiment of inverter circuit according to the present invention is described. As shown in FIG. 1, an inverter circuit of the embodiment is configured by connecting a plurality of unit inverters INV1, INV2, ..., INVn in parallel between an input terminal Vin and an output terminal Vout.

[0007] Each unit inverter is a C-MOS inverter configured by serially connecting a pMOS type FET and nMOS type FET as shown in FIG. 2. Threshold voltage Vin of single C-MOS inverter is expressed in the following Equation (1), assuming a source voltage which is applied to a pMOS type FET to be VDD; a threshold voltage of the pMOS type FET, Vtp; and a threshold voltage of the nMOS type FET, Vtn. On the other hand, when n inverters are connected in parallel, the threshold voltage Vin is given in the following Equation (2).

[0008]

[Equation 1]

$$Vin = (VDD + Vtp + Vtn\sqrt{\beta n / \beta p})/(1 + \sqrt{\beta n / \beta p}) \qquad (1)$$

$$\sum \beta pi(Vin - VDD - Vtpi)^2 = \sum \beta ni(Vin - Vtni)^2 \qquad (2)$$

[0009] Note that βp and βn are coefficients expressed by the following Equations (3) and (4), assuming mobility of electron in the pMOS type FET and the nMOS type FET

to be μp and μn respectively; a dielectric constant of a gate oxide film per unit area and a thickness thereof, e and tox; a channel width, Wp and Wn; and a channel length, Lp and Ln.

[0010]

[Equation 2]

$$\beta p = \mu p \varepsilon / tox \bullet Wp / Lp \qquad (3)$$

$$\beta p = \mu n \varepsilon / tox \bullet Wn / Ln \qquad (4)$$

[0011] Variations in threshold values appear as a normal distribution by the value of β; however, it is impossible to solve Equation (2) analytically since β of two terms are included in the equation. However, it has been known that performance is improved by connecting bipolar transistors in parallel. In general, it is predicted that each characteristic is averaged to realize a stable performance statistically when elements are connected in parallel.

[0012] The prediction is ensured by an experiment. According to a simulation experiment, dispersion V1 (Vin) of the threshold voltage Vin expressed in Equation (1) is higher than dispersion V2 (Vin) of the threshold voltage Vin expressed in Equation (2).

[0013] FIG. 3 is a graph showing voltage characteristics of the inverter circuit in which two unit inverters are connected in parallel. In the graph, a voltage applied to an input terminal Vin is indicated with □-□ line; each characteristic of the respective unit inverters, △-△ line and ▽-▽ line; and characteristics of an inverter circuit in which the two unit inverters are connected in parallel, ○-○ line.

[0014] As is apparent from FIG. 3, by connecting the two unit inverters in parallel, averaged characteristics of the characteristics of the respective inverters can be obtained. The description above also appears in the case where the number of the unit inverters are set 3 or more, for example. Accordingly, by connecting a plurality of unit inverters, precision of the threshold value can be improved statistically, compared to the case of using single unit inverter.

[0015] FIG. 4 shows an arrangement of unit inverters for configuring two inverter circuits by using a plurality of unit inverters of two groups. FIG. 5 shows an equivalent circuit of FIG. 4 to illustrate each inverter circuit clearly. Each inverter circuit is configured by connecting 12 unit inverters a1 to a12 and b1 to b12 in parallel, an input and output terminals of a1 to a12 output Vin1 and Vout1, respectively, and an input and output terminals of b1 to b12 are Vin2 and Vout2, respectively.

[0016] In the arrangement of FIG. 4, a unit inverter of one inverter circuit and a unit inverter of the other inverter circuit are arranged linearly in an alternate manner. Thus, corresponding unit inverters of the two inverter circuits, for example, a1 and b1 or a2 and b2 are disposed adjacently. Generally, in LSI, elements formed in the same pattern and disposed closely have the same characteristics substantially; therefore, these inverter pairs have the same characteristics substantially. By disposing such unit inverters having substantially the same characteristics in parallel, characteristics of first and second inverter circuits can be extremely similar, and an error with design value can also be small along with an effect of relieving variations.

[0017] FIG. 6 shows an arrangement of unit inverters for configuring two systems of circuits configured by connecting three-staged inverter circuits through a junction capacitor by two-stage connection. Referring to equivalent circuit thereof in FIG. 7, in the first system thereof, a first three-staged inverter is configured by serially connecting a first stage in which unit inverters a11, a12, a13 and a14 are connected in parallel, a second stage in which unit inverters b11, b12, b13 and b14 are connected in parallel, and a third stage in which unit inverters c11, c12, c13 and c14 are connected in parallel. Additionally, a second three-staged inverter is configured by serially connecting a first stage in which unit inverters d11, d12, d13 and d14 are connected in parallel, a second stage in which unit inverters e11, e12, e13 and e14 are connected in parallel, and a third stage in which unit inverters f11, f12, f13 and f14 are connected in parallel, and an output of the first three-staged inverter is connected to the second three-staged inverter through a junction capacitor CC1. On the other hand, in the second system, a first three-staged inverter is configured by serially connecting a first stage including parallel unit inverters a21, a22, a23 and a24, a second stage including

parallel unit inverters b21, b22, b23 and b24 and a third stage including parallel unit inverters c21, c22, c23 and c24. A second three-staged inverter is configured by serially connecting a first stage including parallel unit inverters d21, d22, d23 and d24, a second stage including parallel unit inverters e21, e22, e23 and e24 and a third stage including parallel unit inverters f21, f22, f23 and f24. In addition, the first three-staged inverter is connected to the second three-staged inverter through a junction capacitor CC2. Here, FIG. 6 does not show the junction capacitor, but shows only junction terminals C11 and C12 for the junction capacitor CC1 and junction terminals C21 and C22 for the junction capacitor CC2. Note that input and output terminals of the first system are Vin1 and Vin2, respectively, and input and output terminals of the second system are Vin2 and Vout2, respectively.

[0018] As for the arrangement in FIG. 6 for configuring the above-mentioned circuits, in the inverter circuit of the first stage in the first three-staged inverter, the unit inverters a11 to a14 in the first system and the unit inverters a21 to a24 in the second system are disposed alternately, and corresponding unit inverters are disposed adjacently. In addition, input and output terminals of a11 to a14 and a 21 to a 24 are connected respectively in parallel; therefore, variations in characteristics are restrained. In the second stage, the unit inverters of both the systems are alternately arranged while reversing the order of the first and second systems. In other words, the unit inverters b21 to b 24 of the second system and the unit inverters b11 to b14of the first system are arranged alternately, corresponding unit inverters are adjacently disposed, and a plurality of unit inverters are connected in parallel. In the third stage, a relation between the first system and the second system gets back to the state of the first stage. Thus, as a whole, the unit inverters of the first and second systems are arranged in zigzag. According to such configuration, the effect similar to that of the configuration in FIG. 4 can be obtained. In the second three-staged inverter, the alternate arrangement and zigzag arrangement similar to those in the first three-staged inverter are carried out. Similarly to the first three-staged inverter, equalization of characteristics of both the systems and improvement in precision are realized.

[0019] FIG. 8 shows an arrangement of unit inverters for configuring a three-staged

inverter of four systems. Referring to an equivalent circuit in FIG. 9, the first system thereof is formed by serially connecting a first stage in which unit inverters a11, a12, a13 and a14 are connected in parallel, a second stage in which unit inverters b11, b12, b13 and b14 are connected in parallel, and a third stage in which unit inverters c11, c12, c13 and c14 are connected in parallel. The second system is formed by serially connecting a first stage including parallel unit inverters a21, a22, a23 and a24, a second stage including parallel unit inverters b21, b22, b23 and b24 and a third stage including parallel unit inverters c21, c22, c23 and c24. The third system is formed by serially connecting a first stage including parallel unit inverters a31, a32, a33 and a34, a second stage including parallel unit inverters b31, b32, b33 and b34 and a third stage including parallel unit inverters c31, c23, c33 and c34. The fourth system is formed by serially connecting a first stage including parallel unit inverters a41, a42, a43 and a44, a second stage including parallel unit inverters b41, b42, b43 and b44 and a third stage including parallel unit inverters c41, c42, c43 and c44. Here, input and output terminals of the first to the fourth systems are denoted with reference symbols Vin1 and Vin1, Vin2 and Vout2, Vin3 and Vout3, and Vin4 and Vout4, respectively.

[0020] As for an arrangement in FIG. 9 for configuring the above-mentioned circuits, in the inverter circuit of the first stage, the unit inverters a11 to a14 of the first system and the unit inverters a21 to a24 of the second system are connected linearly and alternately. In addition, the unit inverters a 31 to a 34 the third system and the inverters a 41 to a 44 of the forth system are disposed linearly and alternately. Further, rows of the first and second systems and rows of the third and fourth are adjacently disposed, and corresponding unit inverters, for example a11, a21, a31 and a41 are closely disposed with the positional relationship of right, left, top and bottom. As for the second and third stages, arrangement in a similar position is carried out. Thus, as a whole, equalization of characteristics by closely arranging corresponding unit inverters of different systems and improvement in precision by disposing a plurality of unit inverters in parallel are realized.

[0021]

[Effect of the Invention] As described above, according to the present invention,

variations in characteristics of individual unit inverters are absorbed to realize an inverter circuit having a statistically stable performance by using a plurality of unit inverters connected in parallel. In addition, by closely disposing corresponding unit inverters of different inverter circuits, the characteristics of the inverter circuits can be equalized.

[Brief Description of the Drawings]

[FIG. 1] A diagram showing an embodiment of an inverter circuit in accordance with the present invention.

[FIG. 2] A circuit diagram showing a unit inverter used for a circuit shown in FIG. 1

[FIG. 3] A graph showing voltage characteristics of two unit inverters and voltage characteristics of a circuit formed by connecting the two unit circuits in parallel.

[FIG. 4] A circuit diagram (plan diagram) showing an arrangement of unit inverters for two inverter circuits.

[FIG. 5] A circuit diagram showing an equivalent circuit of a circuit shown in FIG. 4.

[FIG. 6] A circuit diagram (plan diagram) showing an arrangement of unit inverters for configuring two systems of circuit formed by serially connecting two three-staged inverter circuits.

[FIG. 7] A circuit diagram showing an equivalent circuit of a circuit shown in FIG. 6.

[FIG. 8] A circuit diagram (plan diagram) showing an arrangement of unit inverters for configuring four systems of three-staged inverter circuits.

[FIG. 9] A circuit diagram showing an equivalent circuit of a circuit shown in FIG. 8.

[Description of the Reference Symbols]

INV1, INV2, ..., INVn: inverters

Vin, Vin1, Vin2, Vin3 and Vin4: input terminals

Vout, Vout1, Vout2, Vout3 and Vout4: output terminals

a11 to a14, a21 to a24, a31 to a34, a 41 to a44, b11 to b14, b21 to b24, b31 to b34, b41 to b44, c11 to c14, c21 to c24, c31 to c34, c41 to c44, d11 to d14, d21 to d24, d31 to d34, d41 to d44, e11 to e14, e21 to e24, e31 to e34, e41 to e44, f11 to f14, f21 to f24, f31 to f34 and f41 to f44 : unit capacitor.

[Amendment]

[Submission Date] November 24, 1995

[Amendment 1]

[Document to be Amended] Specification

[Item to be Amended] Description of the Reference Symbols

[Method of Amendment] Modification

[Contents of Amentment]

[Description of the Reference Symbols]

INV1, INV2, ..., INVn: inverters

Vin, Vin1, Vin2, Vin3 and Vin4: input terminals

Vout, Vout1, Vout2, Vout3 and Vout4: output terminals

a11 to a14, a21 to a24, a31 to a34, a41 to a44, b11 to b14, b21 to b24, b31 to b34, b41 to b44, c11 to c14, c21 to c24, c31 to c34, c41 to c44, d11 to d14, d21 to d24, d31 to d34, d41 to d44, e11 to e14, e21 to e24, e31 to e34, e41 to e44, f11 to f14, f21 to f24, f31 to f34 and f41 to f44: unit capacitor.

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